Low Power Consumption in Symmetric DG Junctionless MOSFET Device with High-K Material Gate Spacer

Ehab F. Hadi[1], Ameer F.Roslan[1], F.Salehuddin[1,*], A.S.M.Zain[1], K.E.Kaharudin[1], Afifah Maheran A.H.[1], A.R.Hanim[1], H.Hazura[1], S.K.Idris[1], I.Ahmad[2]

[1] Micro and Nano Electronics (MiNE), CeTRI, Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia
[2]College of Engineering, Universiti Tenaga Nasional (UNITEN)

[*]Corresponding e-mail: fauziyah@utem.edu.my

ABSTRACT – Double Gate (DG) MOSFET is less sensitive to short channel effect (SCE) due to electrostatic channel control from both sides. Unfortunately, there have been many drawbacks to the normal junction, specifically the inversion junction mode. The Symmetric Junctionless DG-MOSFET device concept has been used to overcome this problem. The simulation result used in SILVACO-ATLAS shows that the proposed device is more immune to SCE because it has a longer effective channel length than the physical length. This device has no junctions and contains the same doping gradients. That's why it's thought to be simpler manufacturing process, better electrical properties and low power consumption than conventional inversion mode devices.

Keywords: *DG-Junctionless; High-K Material*

1. INTRODUCTION

Metal-oxide - semiconductor field effect transistor (MOSFET) device dimensions have been constantly reduced over the past few decades to achieve improved microprocessor speed and storage capacity. Scaling down has made the short channel effect (SCEs) a serious thread on device performance [1,2]. These problems can be solved by using multiple gate or double gate (DG) structures that greatly enhance device electrostatic integrity and thus extend conventional MOSFET's scaling limit. DG MOSFET is less sensitive to SCEs because of electrostatic channel control from both sides. Unfortunately, there have been many drawbacks in the normal junction, specifically inversion junction mode. That's why; the Symmetric Double Gate Junctionless (DGJL) MOSFET device as shown in Figure 1 has been introduced to address this issue [3].

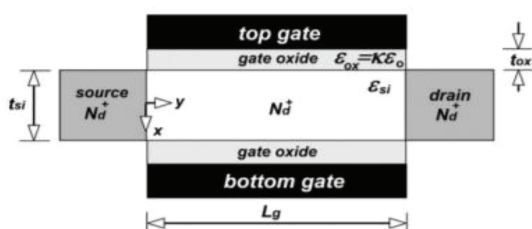

Figure 1. Double Gate Junctionless structure

This device has many advantages over conventional MOSFETs such as high scalability, simple process flow, low thermal budget, improved performance against short-circuit effects [4]. In this paper, a DGJL-MOSFET 16 nm physical channel length has been recoded and a comparison with the inversion mode has been made. The parameters of DGJLMOSFET output including threshold voltage (V_{TH}), slope (SS) and ratio of current (I_{ON}/I_{OFF}) are systematically tested by comprehensive device simulations. For high-k material as a gate spacer, Titanium Oxide (TiO_2) has been chosen. It has been observed that TiO_2 material has an excellent capability of enhancing the device performance with the suppression of SCEs [5,6].

2. MATERIALS AND METHODS

The DG-MOSFET inversion mode consists of two PN-Junctions: source-channel and drain-channel junctions on the source-channel drain direction. The separation between the two joints is called the effective channel length. There is no PN-Junction on the source-channel-drain direction in a DGJL-MOSFET [2]. Therefore, the present driving mechanism in a DGJL-MOSFET is special. Device electrical characteristics are simulated by using SILVACO-ATLAS. For simulations, various variable parameters are gate voltage and gate length which maintain a constant voltage from drain and doping concentration. Uniform doping concentrations in the channel and the source / drain regions are considered for all simulations. Such simulations were carried out by two carriers: the drift-dissemination model with no ionization of effect, the doping dynamic mobility of carriers and the electrical field model of carriers [6,7].

3. RESULT AND DISCUSSION

Table 1 shows the electrical characteristics of the devices. In the subthreshold region, a DGJL-MOSFET is fully depleted, so leakage current is lesser as compared to inversion mode devices. DGJL-MOSFET also shows higher current as compared to DG-MOSFET. High-k dielectric is extensively used for nanoscale device performance improvement, due to its reduced off state leakage and enhanced electrostatic

control over the channel [8,9]. Therefore, in this research, the high-k material from TiO_2 as the gate spacer was used. All the devices are set to the same level of V_{TH} during the simulation which was 0.179V as predicted by ITRS 2013 for High Performance multi-gate technology in the year 2015 [10] at low power supply voltage equal to 0.83V. This is done to precisely evaluate the performance in terms of the corresponding I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, and SS of the device.

Table 1 Comparison between the simulation of three different device

Parameter	**ITRS Predict [10]**	**DG**	**DGJL**	**DGJL with TiO_2 as gate spacer**
V_{TH} (V)	0.179± 12.7%	0.1791	0.1792	0.1791
I_{ON} (µA/µm)	≥1700	1630.79	1684.65	1796.19
I_{OFF} (nA/µm)	≤100	68.58	66.46	65.11
SS (mV/dec)	70~90	93.62	93.53	92.24
I_{ON}/I_{OFF} ratio	≥17000	23779.4	25348.3	27587.0

DGJL-MOSFET device have different enhancements like no junctions, contains same doping gradients so they are thought to be simpler fabrication process, less variability and better electrical property than classical inversion mode devices [11]. The I_{ON}/I_{OFF} ratio is the important figure of merit that indicates the ratio of total I_{ON} to the I_{OFF}. The I_{ON}/I_{OFF} ratio represents the power consumption of a device. The higher I_{ON}/I_{OFF} ratio is, the better power consumption of the device will be [7,8].

4. CONCLUSION

In conclusion, based on the electrical characteristic analysis, the DGJL-MOSFET system has identified good electrical properties such as high drive current and low leakage current. The TiO_2 meanwhile, has resulted in the improvement of the device due to high in current drive which is used to decide on the drive capability of DGJL-MOSFET device. This device with TiO_2 material as a gate spacer also has a better power consumption than any the other device due to its higher I_{ON}/I_{OFF} ratio. In addition, the system features met the high-performance (HP) multi-gate (MG) development specifications expected by ITRS specifications.

ACKNOWLEDGEMENT

The authors would like to thank to the Micro and Nano Electronics (MiNE), CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project

REFERENCES

[1] Ratul Kumar Baruah, Roy P. Paily, "Double-gate junctionless transistor for low power digital applications", International Conference on Emerging Trends and Applications in Computer Science (ICETACS), pp. 23-26, 2013.

[2] Nor Fareza Kosmani, Fatimah A. Hamid, M. Anas Razali, "Effects of High-k Dielectric Materials on Electrical Performance of Double Gate and Gate-All-Around MOSFET", *International Journal of Integrated Engineering*, vol. 12, no. 2, pp. 81-88, 2020.

[3] S. Rai, "Reliability analysis of Junction-less Double Gate (JLDG) MOSFET for analog/RF circuits for high linearity applications", *Microelectronics Journal. Elsevier*, vol. 64, no. 3, pp. 60-68, 2017.

[4] B. Singh, et al., "Analytical Modeling of Channel Potential and Threshold Voltage of Double-Gate Junctionless FETs with a Vertical Gaussian-Like Doping Profile", *IEEE Transactions on Electron Devices*, vo. 63, no. 6, pp. 2299–2305, 2016.

[5] S. Lokman, et. al., "Performance analysis of 19nm n-channel MOSFET device with different high-K dielectric materials", *Proceedings of Mechanical Engineering Research Day 2017*, pp. 86-87, 2017.

[6] S. Chatterjee, A. Chattopadhyay and G. S. Taki, "Characteristics study of high-K gate stack for MOS-FETs using TCAD simulation" *2018 2nd International Conference on Electronics, Materials Engineering and Nano-Technology,* pp. 1-6, 2018

[7] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, A. F. Roslan, "Geometric and process design of ultra-thin junctionless double gate vertical MOSFETs", *International Journal of Electrical and Computer Engineering*, vol. 9, no. 4, pp. 2863-2873, 2019.

[8] A. Nandi, and N. Pandey, "Accurate analytical modeling of junctionless DG-MOSFET by green's function approach", *Superlattices and Microstructures. Elsevier*, vol. 111, pp. 983–990, 2017.

[9] A. F. Roslan, F. Salehuddin, A. S. M. Zain, K. E. Kaharudin, I. Ahmad, "Enhanced performance of 19 single gate MOSFET with high permittivity dielectric material", *Indonesian Journal of Electrical Engineering and Computer Science,* vo. 18, no. 2, pp. 724-730, 2020.

[10] ITRS (2013). *www.ITRS2013.net*

[11] M. Gupta and A. Kranti, "Hysteresis free sub-60 mV/dec subthreshold swing in junctionless MOSFETs", *Proceedings of the IEEE International Conference on VLSI Design*, pp. 133–138, 2018.